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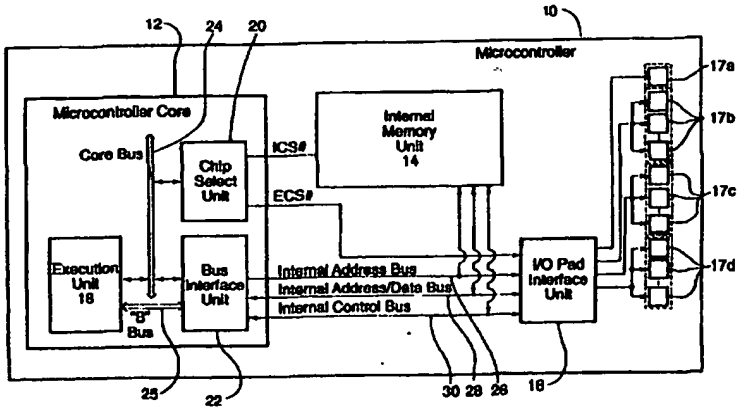

(57) Abstract

A microcontroller is presented which includes a microcontroller core, an internal memory unit, an I/O pad interface unit, and several I/O pads, all formed on a single monolithic silicon substrate. The internal memory unit is configured to store data. A chip select unit within the microcontroller core generates a dedicated internal chip select (ICS#) signal which enables storage operations within the internal memory unit. Key operating parameters of the internal memory unit are stored in a single programmable internal memory chip select register (IMCSR) located within the chip select unit. The size of the internal memory unit is fixed, eliminating the need to store size information. The internal memory chip select register contains a base address field. The base address field includes a minimum number of the highest-ordered bits of a base address of the internal memory unit required to define which non-overlapping section of the physical address space the internal memory unit is mapped into. The method of accessing the internal memory unit allows backwards compatibility with existing microcontroller products. The microcontroller core also includes an execution unit and a bus interface unit. The execution unit executes microprocessor instructions, preferably instructions from an x86 instruction set. The bus interface unit handles all data transfer operations for the microcontroller core in accordance with established protocols. The I/O pad interface unit provides the microcontroller with off-chip data transfer capability, allowing the microprocessor to read data from or write data to external devices.

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TITLE: A MICROCONTROLLER INCLUDING AN INTERNAL MEMORY UNIT AND CIRCUITRY TO GENERATE AN ASSOCIATED ENABLE SIGNAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the manufacture of integrated circuits and more particularly to the manufacture of microcontrollers.

2. Description of the Relevant Art

A typical computer system includes a microprocessor secured within its own semiconductor device package. Several separately-packaged support circuits are connected to the microprocessor. These support circuits perform support functions including communication functions and memory interface functions. A microcontroller is an integrated circuit which incorporates a microprocessor core along with one or more support circuits on the same monolithic semiconductor substrate (i.e., chip). Computer systems which employ microcontrollers may thus be formed using fewer semiconductor devices. Advantages of such systems include lower fabrication costs and higher reliabilities. Microcontrollers find applications in industrial and commercial products including control systems, computer terminals, hand-held communications devices (e.g., cellular telephones), photocopier machines, facsimile machines, and hard disk drives.

The 80186 and 80188 microcontrollers were first introduced in the early 1980's. The 80186 microcontroller contains 16-bit registers and functional units which communicate via a 16-bit internal data bus. The 80186 microcontroller has 16 data exchange terminals which may be connected to devices external to the microcontroller. The 80188 microcontroller also has 16-bit internal registers and a 16-bit internal data bus, but has only 8 data exchange terminals.

In a typical computer system, a memory subsystem includes a memory interface unit and one or more separately-packaged memory devices. The memory interface unit is coupled between the microprocessor and the memory devices, and generates control signals required to store data within and retrieve stored information from the memory devices. Each of the memory devices includes a chip select terminal coupled to receive a chip select signal generated by the memory interface unit. Memory devices which are active during a given memory access receive an asserted chip select signal.

The 80186 and 80188 microcontrollers incorporate the functions of the memory interface unit, thus eliminating the need for the memory interface unit and allowing the one or more separately-packaged memory devices to be directly connected to the microcontroller. A chip select unit within 80186 and 80188 microcontrollers generates several different chip select signals. Each chip select signal is typically associated with a defined section of a physical memory space of the microcontroller. Each chip select signal is driven

upon a dedicated terminal located on the microcontroller package (e.g., a package pin). A chip select terminal of a separately-packaged memory device is connected to a particular chip select terminal of the microprocessor, thus enabling the memory device when a memory access occurs within the section of the physical address space associated with the chip select signal. In addition, the 80186 microcontroller includes a bus interface unit which generates a signal to indicate which 8-bit byte of a 16-bit value present on its 16 data exchange terminals is active during a given memory access operation.

The 80186 and 80188 microcontrollers have 20 address pins, and may thus generate 2^{20} unique memory addresses. As a result, the 80186 and 80188 microcontrollers may access 2^{20} unique memory locations (i.e., 1,048,576 8-bit bytes of memory, or a 1 Mbyte physical address space). As with all x86 microprocessors, the 80186 and 80188 microcontrollers begin fetching instructions at memory location FFFF0h near the uppermost portion of the 1 Mbyte physical address space following assertion of a reset signal. Assertion of the reset signal is typically used to initialize the microprocessor immediately following the application of electrical power. The reset signal initiates a "boot" sequence. The contents of any volatile memory device including location FFFF0h (i.e., mapped into the uppermost portion of the physical address space) would be unreliable following an interruption in power, thus one or more non-volatile memory devices are typically mapped into the uppermost portion of the physical address space. Such non-volatile memory devices include various types of read only memory (ROM) devices.

In addition, a section of the lowermost portion of the address space is dedicated to operating system functions. An operating system is a collection of software programs which provide file management, input/output control, and a controlled environment for executions of applications programs. MS-DOS® and Windows NT™ (Microsoft Corp.) are common operating systems. An application program is a computer program which performs a specific function and is designed to operate within a controlled environment provided by an operating system. During system initialization, a typical operating system loads an interrupt vector table into the lowermost 1,024 (1k) bytes of memory starting at memory location 00000h. The interrupt vector table contains the starting addresses of interrupt service routines which handle interrupts arising from devices arranged external to the microcontroller. An external interrupt may originate from a peripheral device which is ready to transmit data to or receive data from the microcontroller (i.e., requires servicing by the microcontroller). The interrupt service routines themselves are also typically stored in the lowermost portion of the memory address space (i.e., the portion of the address space including location 00000h), along with data and other routines used by the operating system. Examples of data needed by the operating system include memory addresses assigned to various peripheral devices. The routines and data needed by the operating system may be loaded into volatile memory from an external source during system initialization, or may be permanently stored in non-volatile memory mapped to the lowermost portion of the address space. The section of the lowermost portion of the address space dedicated to operating system functions is not available for use by application programs.

As a direct result of the above system requirements, the memory address spaces of the 80186 and 80188 microcontrollers are partitioned into an upper memory address area, a lower memory address area, and a midrange memory address area. The upper memory address area is bounded at a high end by address FFFFFh,

the highest address in the physical address space. The upper memory address area typically includes one or more non-volatile memory devices containing microprocessor initialization instructions. The chip select unit generates a single upper memory chip select signal for the one or more memory devices located within (i.e., mapped into) the upper memory address area.

The lower memory address area is bounded at a low end by address 00000h, the lowest address in the physical address space. As described above, a section of the lower memory address area is dedicated to the operating system. The lower memory address area may include one or more volatile memory devices, or may include one or more non-volatile memory devices containing operating system data and routines. The chip select unit generates a single lower memory chip select signal for the one or more memory devices mapped into the lower memory address area.

The midrange memory address area is located between the upper and lower memory address areas, and is available for application programs and associated data. A single memory block, consisting of from 8k to 512k bytes of contiguous memory, may be mapped into the bounds of the midrange memory address area. This memory block may be divided into four sections. The chip select unit is capable of generating up to four midrange memory chip select signals, one for each memory block section. Each midrange memory chip select signal may be used to enable one or more devices mapped into a given memory block section.

Finite amounts of time are required to transfer data between a microcontroller and an external memory device. Systems with higher performance levels must accomplish such transfers in shorter amounts of time. In general, the amount of time required to accomplish such a transfer depends upon the speed of the memory device and the distance between the microcontroller and the memory device. Faster memory devices are able to retrieve and store data in shorter periods of time. Such faster memory devices typically cost more than slower memory devices. Signals travel along signal paths at finite speeds, thus taking longer to traverse greater distances. The greater the distance between the microcontroller and the memory device, the greater the signal delay time introduced, and the greater the negative impact upon system performance.

It would thus be advantageous to include one or more memory devices upon the same microcontroller chip. The distance that signals must travel between the microcontroller and the one or more memory devices would be reduced, thus resulting in higher levels of system performance. The increased level of system integration would also result in lower system costs and higher system reliabilities.

SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by a microcontroller formed upon a single monolithic substrate and having an internal memory unit and circuitry to generate an internal memory unit enable signal. As used herein, "internal" is used to describe an element which is part of the microcontroller, and "external" is used to describe an element which not part of the microcontroller. The internal memory unit is configured to store data. A chip select unit of the microcontroller generates a dedicated internal chip select (ICS#) signal which enables storage operations within the internal memory unit. Key operating parameters of the internal memory unit are stored in a single programmable internal memory chip select register located

within the chip select unit. The size of the internal memory unit is fixed, eliminating the need to store size information. The internal memory chip select register contains a base address field. The base address field includes a minimum number of the highest-ordered bits of a base address of the internal memory unit required to define which non-overlapping section of the physical address space the internal memory unit is mapped into. For example, only the 5 highest-ordered bits of a 20-bit base address are required to define which 32 kbyte section of a 2^{20} byte physical address space a 32 kbyte internal memory unit is mapped into. In this case, the base address field of the internal memory chip select register contains only the 5 highest-ordered bits of the base address.

An added benefit of accessing the internal memory unit as described herein is that it allows backwards compatibility with existing microcontrollers. The present microcontroller may be made pin-compatible and software-compatible with existing products. Thus the present microcontroller may be substituted for an earlier version of the microcontroller within an existing system with no required changes to system software. System software modification is only required if a user wishes to take advantage of the presence of the internal memory unit.

Along with the internal memory unit, the microcontroller also includes a microcontroller core, an I/O pad interface unit, and several I/O pads. The chip select unit is located within the microcontroller core, along with an execution unit and a bus interface unit. The execution unit is configured to execute microprocessor instructions, preferably instructions from an x86 instruction set. During the execution of microprocessor instructions, the execution unit generates output data which represent offset portions of addresses of memory locations within a physical address space from which data is to be read or to which data is to be written. The bus interface unit receives the offset portion of the address, combines it with a segment portion, and produces and address signal. The chip select unit receives the address signal and generates the ICS# signal if the address signal corresponds to a memory location within the internal memory unit. If the address signal corresponds to a memory location within an external (i.e., off-chip) memory unit, the chip select unit generates an external chip select (ECS#) signal. The bus interface unit includes multiple data buffers and handles all data transfer operations for the microcontroller core in accordance with established protocols. The I/O pad interface unit provides the microcontroller with off-chip data transfer capability, allowing the microprocessor to read data from or write data to external devices. The I/O pad interface unit contains driver circuits to cause voltages on the I/O pads to correspond to the voltages on the associated internal signal lines (i.e., to drive signals present on internal signal lines onto corresponding I/O pads), and also contains driver circuits to drive signals present on I/O pads onto corresponding internal signal lines.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a preferred embodiment of a microcontroller in accordance with the present invention;

Fig. 2 is a block diagram of a preferred embodiment of an internal memory unit which includes a memory control unit coupled to a memory array;

Fig. 3 is a block diagram of one embodiment of a chip select unit which generates an external chip select (ECS#) signal and an internal chip select (ICS#) signal;

Fig. 4 is a block diagram of one embodiment of an external memory chip select register containing key operating parameters of an external memory unit and used in the generation of the ECS# signal;

Fig. 5 is a block diagram of one embodiment of an external memory auxiliary register containing the size of the external memory unit and used in the generation of the ECS# signal;

Fig. 6 is a block diagram of one embodiment of an internal memory chip select register containing key operating parameters of an internal memory unit and used in the generation of the ICS# signal;

Fig. 7 is a block diagram of a 1 Mbyte physical address space partitioned into sections, each section containing 32 kbytes of memory, wherein the 5 highest-ordered bits of a 20-bit base address define the 32 kbyte section into which the internal memory unit is mapped;

Fig. 8 is an internal bus cycle timing diagram associated with retrieving (i.e., reading) data stored within the memory array of the internal memory unit; and

Fig. 9 is an internal bus cycle timing diagram associated with the saving of data within (i.e., the writing of data to) the memory array of the internal memory unit.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications,

equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 is a block diagram of a preferred embodiment of a microcontroller 10 in accordance with the present invention. Microcontroller 10 includes a microcontroller core 12, an internal memory unit 14, an input/output (I/O) pad interface unit 16, and I/O pads 17 all on a single monolithic semiconductor substrate (i.e., chip). Microcontroller core 12 includes an execution unit 18, a chip select unit 20, and a bus interface unit 22 coupled to a core bus 24. Execution unit 18 executes microprocessor instructions, preferably from an instruction set of an x86 microprocessor. Execution unit 18, chip select unit 20, and bus interface unit 22 communicate via signals driven on signal lines of core bus 24. In addition, execution unit 18 and bus interface unit 22 are "tightly coupled" to one another by a "B" bus 25. As will be described in more detail below, chip select unit 20 is configured to produce an external chip select (ECS#) signal and an internal chip select (ICS#) signal. (Signal names followed by '#' are active low, meaning the signal is active or asserted when the signal voltage corresponds to that of a low logic level). Signal ECS# provides an enable signal for an external (i.e., off-chip) memory unit or an external I/O device (not shown). Signal ICS# is a dedicated internal signal which provides an enable signal for internal memory unit 14. When asserted, signal ICS# enables data storage operations within internal memory unit 14. Bus interface unit 22 handles all data transfers between microcontroller core 12 and internal memory unit 14, and between microcontroller core 12 and external devices such as off-chip memory devices and I/O devices.

In the embodiment of Fig. 1, bus interface unit 22 is coupled to three internal buses: an internal address bus 26, an internal address/data bus 28, and an internal control bus 30. Internal address bus 26 includes multiple signal lines, and each signal line is configured to carry an address signal. Internal address/data bus 28 is a common multiplexed address/data bus. Internal address/data bus 28 includes multiple signal lines, and each signal line is configured to carry an address signal during certain time intervals and a data signal during other time intervals. Such multiplexed buses are used to reduce the total number of required signal lines. Internal control bus 30 includes multiple signal lines, and each signal line is configured to carry a control signal. Bus interface unit 22 contains multiple data buffers and is configured to generate and drive address, data, and control signals onto internal address bus 26, internal address/data bus 28, and internal control bus 30, respectively, in accordance with established protocols in order to accomplish data transfers as described above.

During manufacture of microcontroller 10, signal lines to be connected to external devices are terminated at flat metal contact regions (i.e., I/O pads) located upon an exposed surface of the chip. Following manufacture, microcontroller 10 is typically secured within a protective semiconductor device package. Each I/O pad is then connected to a terminal (i.e., pin) of the device package by a signal line (i.e., a wire). I/O pad interface unit 16 is coupled between internal signal lines and I/O pads 17. I/O pad interface unit 16 contains driver circuits to cause voltage levels on the I/O pads to correspond to voltage levels on associated internal signal lines (i.e., drive signals present on internal signal lines onto corresponding I/O pads). I/O pad interface

unit 16 also contains driver circuits to drive signals present on I/O pads onto corresponding internal signal lines. In addition, I/O pad interface unit 16 contains logic circuitry to latch (i.e., sample and hold) some internal signals prior to driving them onto corresponding I/O pads. For example, I/O pad interface unit 16 drives signal ECS# onto I/O pad 17a. I/O pad interface unit 16 also drives signals present on the signal lines of internal address bus 26 onto corresponding I/O pads 17b. I/O pad interface unit 16 drives signals present on the signal lines of internal address/data bus 28 onto corresponding I/O pads 17c during certain time intervals, and drives signals present on I/O pads 17c onto corresponding signal lines of internal address/data bus 28 during other time intervals. I/O pad interface unit 16 drives output control signals present on certain signal lines of internal control bus 30 onto corresponding I/O pads 17d, and drives input control signals present on I/O pads 17d onto corresponding signal lines of internal control bus 30.

Internal memory unit 14 is configured to store data. Fig. 2 is a block diagram of a preferred embodiment of internal memory unit 14, including a memory control unit 32 coupled to a memory array 34. Memory control unit 32 is coupled to receive the ICS# signal produced by chip select unit 20, and is also coupled to signal lines of internal address bus 26, internal address/data bus 28, and internal control bus 30. Memory array 34 includes many storage locations (i.e., memory cells). The assertion of the ICS# signal enables storage operations within internal memory unit 14. Memory control unit 32 generates and issues control signals to memory array 34 required to save data within memory array 34 and to retrieve data from memory array 34. As external devices cannot access the contents of the storage locations within internal memory unit 14, memory control unit 32 also preferably includes a built-in self test capability to ensure proper operation of internal memory unit 14.

Memory array 34 preferably includes many high-density dynamic random access memory (DRAM) memory cells. In this case, memory control unit 32 also preferably includes refresh circuitry to provide periodic memory cell refreshing. Alternately, memory array 34 may include many lower density static random access memory (SRAM) memory cells. Other suitable types of memory cells include non-volatile memory cells such as electrically erasable programmable read only memory (EEPROM) cells and flash memory cells. Flash memory devices are sometimes called flash EEPROM devices, and differ from EEPROM devices in that electrical erasure involves large sections of, or the entire contents of, a flash memory device.

Fig. 3 is a block diagram of one embodiment of chip select unit 20. Chip select unit 20 includes logic circuitry used in conjunction with the contents of a programmable external memory chip select register (EMCSR) 36 and a programmable external memory auxiliary register (EMAR) 38 to generate signal ECS#. Chip select unit 20 also includes logic circuitry used in conjunction with a programmable internal memory chip select register (IMCSR) 40 to generate signal ICS#. All three registers are memory-mapped internal registers which may be read or written just like memory locations. Initializations of these registers are accomplished by microprocessor instructions which write desired values to the addresses assigned to the internal registers.

Figs. 4-6 are block diagrams of embodiments of internal registers used with a segmented memory system common to x86 microprocessors. During generation of a 20-bit physical address, execution unit 18 passes a 16-bit "offset" portion of an address to bus interface unit 22 via "B" bus 25. Bus interface unit combines the 16-bit offset portion with a 16-bit "segment" portion of the address via a shift-and-add operation

to form the 20-bit physical address. Bus interface unit 22 contains a 16-bit register which holds the segment portion of the address, and also contains dedicated hardware to perform the shift-and-add operation. During the shift-and-add operation, the 16-bit segment portion of the address is first shifted left four bit positions. Following the left shift operation, the four least-significant bits of the resulting 20-bit segment base address are all zeros. The 16-bit offset portion is then added to the segment base address, and the result is the 20-bit physical address.

The embodiment of EMAR 38 shown in Fig. 5 is similar to the PCS# and MCS# auxiliary register of 80186 and 80188 microcontrollers. Bits 14, 13, 12, 11, 10, 9, and 8 (14-8) of the embodiment of EMAR 38 shown in Fig. 5 specify the size of an external memory unit in bytes as shown in Table 1 below. Bit 15 of EMAR 38 is reserved, and bits 7-0 of EMAR 38 are not used.

Table 1. EMAR Memory Block Size Programming.

EMAR Bits 14-8	Memory Block Size
0000001	8 kbytes
0000010	16 kbytes
0000100	32 kbytes
0001000	64 kbytes
0010000	128 kbytes
0100000	256 kbytes
1000000	512 kbytes

The embodiment of EMCSR 36 shown in Fig. 4 is similar to the mid-range memory chip select register of 80186 and 80188 microcontrollers. Bits 15-9 of the embodiment of EMCSR 36 shown in Fig. 4 define the 7 highest-ordered bits of a 20-bit base address of the external memory unit, BA(19:13). The remaining 13 bits of the base address are always 0. The base address must be an integer multiple of the memory block size in EMAR register 38. For example, if the memory block size is 64 kbytes, bits 15-9 of EMCSR 36 can only be xxxx000, where 'x' is a 0 or a 1. Bits 8-3 of EMCSR 36 are reserved.

Bus interface unit 22 performs read and write (i.e., data transfer) operations in four cycles of a system clock signal. Bus interface unit 22 receives an input "ready" control signal which allows data transfer operations to be extended to more than four cycles. The ready signal is present on a dedicated ready signal line of internal control bus 30. An external device with a connection to an associated I/O pad of I/O pads 17d signals its ready status via the ready signal. If the device is ready, the device asserts the ready signal. The device signals a not-ready condition by deasserting the ready signal. I/O pad interface unit 16 drives the ready signal onto the ready signal line of internal control bus 30. Bus interface unit 22 receives the ready signal via the ready signal line of control bus 30. Bus interface unit 22 samples the ready signal line of internal control bus 30 during the third cycle of a data transfer operation, and responds to a deasserted ready signal by extending the time interval of the data transfer operation by a predetermined number of additional cycles (i.e., inserting a

predetermined number of wait states). The process of inserting wait states is continued until the device asserts the ready signal.

Bit 2 (R2) of EMCSR 36 is the ready mode bit. If the R2 bit is 0, bus interface unit 22 samples the ready signal during the third cycle of a data transfer operation to determine if the device requires the insertion of wait states. If the R2 bit is 1, bus interface unit 22 does not sample the ready signal, and data transfer operations are completed in four cycles. Bits 1 and 0 (R1 and R0) define the number of wait states bus interface unit 22 inserts when the ready signal is deasserted during a data transfer operation.

In order to read data from memory or write data to memory, execution unit 18 drives a 16-bit offset portion of the address of the memory location to be accessed onto signal lines of "B" bus 25. Bus interface unit 22 receives the offset portion of the address and combines it with a 16-bit segment portion to generate a 20-bit physical address as described above. Bus interface unit 22 drives the 20-bit physical address of the memory location to be accessed onto core bus 24. Chip select unit 20 receives the 20-bit physical address from core bus 24, and asserts the ECS# signal if the 7 highest-ordered bits of the 20-bit physical address match the contents of bits 15-9 of EMCSR 36.

Fig. 6 is a block diagram of one embodiment of IMCSR 40. Unlike the external memory unit, the size of internal memory unit 14 is fixed, eliminating the need for a separate register to contain the size information. The embodiment of Fig. 6 corresponds to an internal memory unit 14 having 32k (2^{15}) 8-bit bytes of memory. In order to map internal memory unit 14 into one of several non-overlapping blocks of the physical memory space, the 5 highest-ordered bits of a 20-bit base (i.e., starting) address of internal memory unit 14 must be specified. Thus a 5-bit base address field is defined within IMCSR 40, comprising storage locations 15, 14, 13, 12, and 11 (i.e., bits 15-11). In general, the base address field of IMCSR 40 includes the (m - n) highest-ordered bits of a base address of internal memory unit 14, where a physical address space includes 2^m unique addresses, and internal memory unit 14 includes 2^n memory locations. The 5 highest-ordered bits of the 20-bit base address of internal memory unit 14 are stored in the base address field labeled BA(19:15) in Fig. 6. The remaining 15 bits of the base address are always 0. The base address field of IMCSR 40 thus defines the starting address of a 32 kbyte section of the physical address space into which internal memory unit 14 is mapped. The fact that the highest-ordered bits of IMCSR 40 are used to contain the highest-ordered bits of the base address facilitates address comparisons described below.

Fig. 7 is a block diagram of a 1 Mbyte physical address space divided into 32 kbyte sections. Fig. 7 will be used to illustrate how the base address field of IMCSR 40 defines the 32 kbyte segment into which the 32 kbyte internal memory unit 14 is mapped. First, assume that the storage locations making up the base address field of IMCSR 40 all contain the value 0. Thus bits 19-15 of a base address of internal memory unit 14 are 00000. As mentioned above, the remaining 15 bits of the base address are always 0. The base address of internal memory unit 14 is thus 00000000000000000000, or 00000h. Thus the 32k bytes of memory within internal memory unit 14 span from 00000h to 07FFFh. Now assume that the storage locations making up the base address field of IMCSR 40 contain 00001, respectively. Thus bits 19-15 of a base address of internal memory unit 14 are 00001, the remaining 15 bits of the base address are 0, and the base address of internal memory unit 14 is 00001000000000000000, or 08000h. Thus the 32k bytes of memory within internal memory

unit 14 span from 08000h to 0FFFFh. There are 2^5 or 32 possible non-overlapping, 32-kbyte sections of the physical address space into which internal memory unit 14 may be mapped, and Fig. 7 shows several of them.

Bit 10 of IMCSR 40 is the Show Read (SR) bit. During a read operation involving internal memory unit 14, internal memory unit 14 drives signal lines of internal address/data bus 28 with retrieved data. If the SR bit is 0, I/O pad interface unit 16 does not drive the retrieved data onto the corresponding I/O pads. If the SR bit is 1, I/O pad interface unit 16 drives data the retrieved data onto the corresponding I/O pads. In this case, the data provided by internal memory unit 14 during a read operation is thus made visible on the pins of the device package containing microcontroller 10, and may be useful for debugging purposes. Bit 9 of IMCSR 40 is the Memory Enable (ME) bit. If the ME bit is 0, the ICS# signal is never asserted, thus internal memory unit 14 is disabled. Setting the ME bit to 1 enables assertion of the ICS# signal, thus the operation of internal memory unit 14 is enabled. Generation of the ICS# signal by chip select unit 20 is enabled by establishing the base address of internal memory unit 14 (bits 19-11 of IMCSR 40) and setting the ME bit (bit 9 of IMCSR 40) to 1. Bits 8-0 of IMCSR 40 are reserved for future use.

During read and write operations, execution unit 18 drives the offset portion of the address of the memory location to be accessed onto signal lines of "B" bus 25. Bus interface unit 22 receives the offset portion from the signal lines of "B" bus 25 and combines it with a 16-bit segment portion to generate a 20-bit physical address as described above. Bus interface unit 22 drives the 20-bit physical address of the memory location to be accessed onto core bus 24. Chip select unit 20 receives the 20-bit physical address from core bus 24, and asserts the ICS# signal if: (i) the 5 highest-ordered bits of the 20-bit physical address match the contents of the base address field of IMCSR 40, and (ii) the memory enable bit within IMCSR 40 is set to 1.

Figs. 8 and 9 will be used to describe bus cycles associated with data transfers between microcontroller core 12 and internal memory unit 14. As described above, such transfers typically span four consecutive cycles of a system clock signal CLK. Fig. 8 is an internal bus cycle timing diagram associated with retrieving (i.e., reading) data stored within memory array 34 of internal memory unit 14. During a first cycle 42 of signal CLK, bus interface unit 22 of microcontroller core 12 drives signal lines of internal address bus 26 and internal address/data bus 28 with the address of a memory location within memory array 34 of internal memory unit 14 containing the desired data. Chip select unit 20 also asserts the ICS# signal, enabling data storage operations within internal memory unit 14. Bus interface unit 22 also drives a signal line of internal control bus 30 with a control signal (not shown) which causes memory control unit 32 to latch the address present on the signal lines of internal address bus 26 and internal address/data bus 28. During a second cycle 44 of signal CLK, bus interface unit 22 ceases driving signal lines of internal address/data bus 28 in preparation to receive data over some of the same signal lines during the following cycle. Bus interface unit 22 also drives an asserted read signal RD# on a signal line of internal control bus 30 which causes memory control unit 32 to generate and issue control signals to memory array 34 required to retrieve data from the memory location at the latched address. During a third cycle 46 of signal CLK, memory control unit 32 drives the signal lines of internal address/data bus 28 with the retrieved data. Bus interface unit 22 reads the data driven on the signal lines of internal address/data bus 28 at the falling edge of signal CLK marking the end of third cycle 46. During a fourth cycle 48, memory control unit 32 ceases driving signal lines of internal address/data bus 28 in

preparation to receive address information over some of the same signal lines during the following cycle. Bus interface unit 22 deasserts the ICS# and RD# signals.

Fig. 9 is an internal bus cycle timing diagram associated with the saving of data within (i.e., the writing of data to) memory array 34 of internal memory unit 14. During a first cycle 50 of signal CLK, bus interface unit 22 of microcontroller core 12 drives signal lines of internal address bus 26 and internal address/data bus 28 with the address of a memory location within memory array 34 in which data is to be saved. Chip select unit 20 also asserts the ICS# signal, enabling data storage functions within internal memory unit 14. Bus interface unit 22 also drives a signal line of internal control bus 30 with a control signal (not shown) which causes memory control unit 32 to latch the address present on the signal lines of internal address bus 26 and internal address/data bus 28. During a second cycle 52 of signal CLK, bus interface unit 22 drives an asserted write signal WR# on a signal line of internal control bus 30, causing memory control unit 32 to prepare to store data within memory array 34. During a third cycle 54 of signal CLK, bus interface unit 22 deasserts the WR# signal, causing memory control unit 32 to read the data on the signal lines of internal address/data bus 28, and to generate and issue control signals to memory array 34 required to save the data in the memory location at the latched address. During a fourth cycle 56, bus interface unit 22 deasserts the ICS# signal.

Memory control unit 32 of internal memory unit 14 is coupled to the ready signal line of internal control bus 30. As mentioned above, bus interface unit 22 always samples the ready signal line of internal control bus 30 during the third cycle of a read or write operation. If internal memory unit 14 is ready, it asserts the ready signal. Internal memory unit 14 signals a not-ready condition by deasserting the ready signal. If the ready signal is deasserted by internal memory unit 14 during the third cycle of a read or write operation, bus interface unit 22 inserts a single wait state. The process of inserting a wait state is continued until internal memory unit 14 asserts the ready signal. The ready signal is used to allow an occasional delay in memory access without requiring that all memory accesses be delayed. Such occasional delays may occur when memory array 34 of internal memory unit 14 includes DRAM memory and the memory location being accessed is undergoing a DRAM refresh operation.

It will be appreciated by those skilled in the art having the benefit of this disclosure that this invention is believed to be a microcontroller formed upon a single monolithic semiconductor substrate and including an internal memory unit and circuitry to generate an associated internal memory unit enable signal. Furthermore, it is also to be understood that the form of the invention shown and described is to be taken as exemplary, presently preferred embodiments. Various modifications and changes may be made without departing from the spirit and scope of the invention as set forth in the claims. It is intended that the following claims be interpreted to embrace all such modifications and changes.

WHAT IS CLAIMED IS:

1. A microcontroller formed upon a single monolithic semiconductor substrate, comprising:

an execution unit for producing output data in response to an instruction;

a bus interface unit coupled to the execution unit and configured to produce an address signal in response to the output data;

a chip select unit coupled to receive the address signal and configured to produce an internal memory select signal and an external memory select signal in response to the address signal;

an internal memory configured to store data, wherein the internal memory is responsive to the address signal during assertion of the internal memory select signal; and

an output pad responsive to the external memory select signal.

2. The microcontroller as recited in claim 1, further comprising a core bus interconnected between the execution unit, the chip select unit, and the bus interface unit.

3. The microcontroller as recited in claim 1, wherein the execution unit is configured to execute instructions arising from an x86 instruction set.

4. The microcontroller as recited in claim 1, wherein the output data produced by the execution unit comprises an offset portion of the address signal.

5. The microcontroller as recited in claim 4, wherein the chip select unit comprises a programmable internal memory select register, and wherein the internal memory select register comprises a first plurality of bit locations which define a base address of the internal memory.

6. The microcontroller as recited in claim 5, wherein the programmable internal memory select register further comprises a memory enable bit location which defines whether to enable the internal memory.

7. The microcontroller as recited in claim 6, wherein the chip select unit asserts the internal memory enable signal if: (i) the highest-ordered bits of the address signal match the contents of the first plurality of bit locations, and (ii) the memory enable bit location contains the value 1.

8. The microcontroller as recited in claim 4, wherein a physical address space comprises 2^m unique addresses, the internal memory comprises 2^n memory locations, and the first plurality of bit locations comprises $(m - n)$ consecutive bit locations.

9. The microcontroller as recited in claim 8, wherein the first plurality of bit locations are the highest-ordered bit locations within the internal memory chip select register.

10. The microcontroller as recited in claim 5, wherein the microcontroller employs segmented addressing in which a 16-bit segment value is combined with a 16-bit offset value to form a 20-bit physical address, and the internal memory chip select register comprises 16 bit locations.

11. The microcontroller as recited in claim 10, wherein a physical address space comprises 2^{20} unique addresses, the internal memory comprises 2^n memory locations, and the first plurality of bit locations comprises $(20 - n)$ consecutive bit locations.

12. The microcontroller as recited in claim 11, wherein the first plurality of bit locations are the highest-ordered bit locations within the internal memory chip select register.

13. The microcontroller as recited in claim 10, wherein the internal memory comprises 2^{15} memory locations, and the first plurality of bit locations comprises 5 consecutive bit locations.

14. The microcontroller as recited in claim 13, wherein the first plurality of bit locations are the highest-ordered bit locations within the internal memory chip select register.

15. The microcontroller as recited in claim 14, wherein one of the bit locations of the internal memory chip select register is a memory enable bit location which defines whether to enable the internal memory.

16. The microcontroller as recited in claim 15, wherein the chip select unit asserts the internal memory enable signal if: (i) the 5 highest-ordered bits of the address signal match the contents of the first plurality of bit locations, and (ii) the memory enable bit location contains the value 1.

17. A microcontroller formed upon a single monolithic semiconductor substrate, comprising:

a microcontroller core, comprising:

an execution unit configured to execute instructions and to produce output data;

a bus interface unit coupled to receive the output data from the execution unit and configured to produce an address signal; and

a chip select unit coupled to receive the address signal and configured to produce an external memory enable signal and an internal memory enable signal;

an internal memory unit coupled to receive the address and internal memory enable signals and configured to store data, wherein the internal memory unit is responsive to the address signal during assertion of the internal memory enable signal;

an I/O pad; and

an I/O pad interface unit coupled to receive the external memory enable signal and configured to drive the external memory enable signal onto the I/O pad.

18. The microcontroller as recited in claim 17, wherein the execution unit is configured to execute instructions from an x86 instruction set.

19. The microcontroller as recited in claim 17, wherein the output data produced by the execution unit is an offset portion of a memory address.

20. The microcontroller as recited in claim 19, wherein the chip select unit comprises a programmable internal memory chip select register, wherein the internal memory chip select register comprises a plurality of bit locations organized in a linear arrangement.

21. The microcontroller as recited in claim 20, wherein the internal memory chip select register comprises a base address field, wherein the base address field is a contiguous subset of the plurality of bit locations configured to store a corresponding number of the highest-ordered bits of a base address of the internal memory unit.

22. The microcontroller as recited in claim 21, wherein the microcontroller employs segmented addressing in which a 16-bit segment value is combined with a 16-bit offset value to form a 20-bit physical address, and the internal memory chip select register comprises 16 bit locations.

23. The microcontroller as recited in claim 22, wherein the internal memory unit comprises 2^{15} memory locations, and the base address field of the internal memory chip select register comprises 5 bit locations.

24. The microcontroller as recited in claim 23, wherein the 5 bit locations of the base address field are the highest-ordered bit locations within the internal memory chip select register.

25. The microcontroller as recited in claim 24, wherein one of the bit locations of the internal memory chip select register is a memory enable bit location which defines whether to enable the internal memory.

26. The microcontroller as recited in claim 25, wherein the chip select unit asserts the internal memory enable signal if: (i) the 5 highest-ordered bits of the segment portion of the memory address match the contents of the 5 bit locations of the base address field, and (ii) the memory enable bit location contains the value 1.

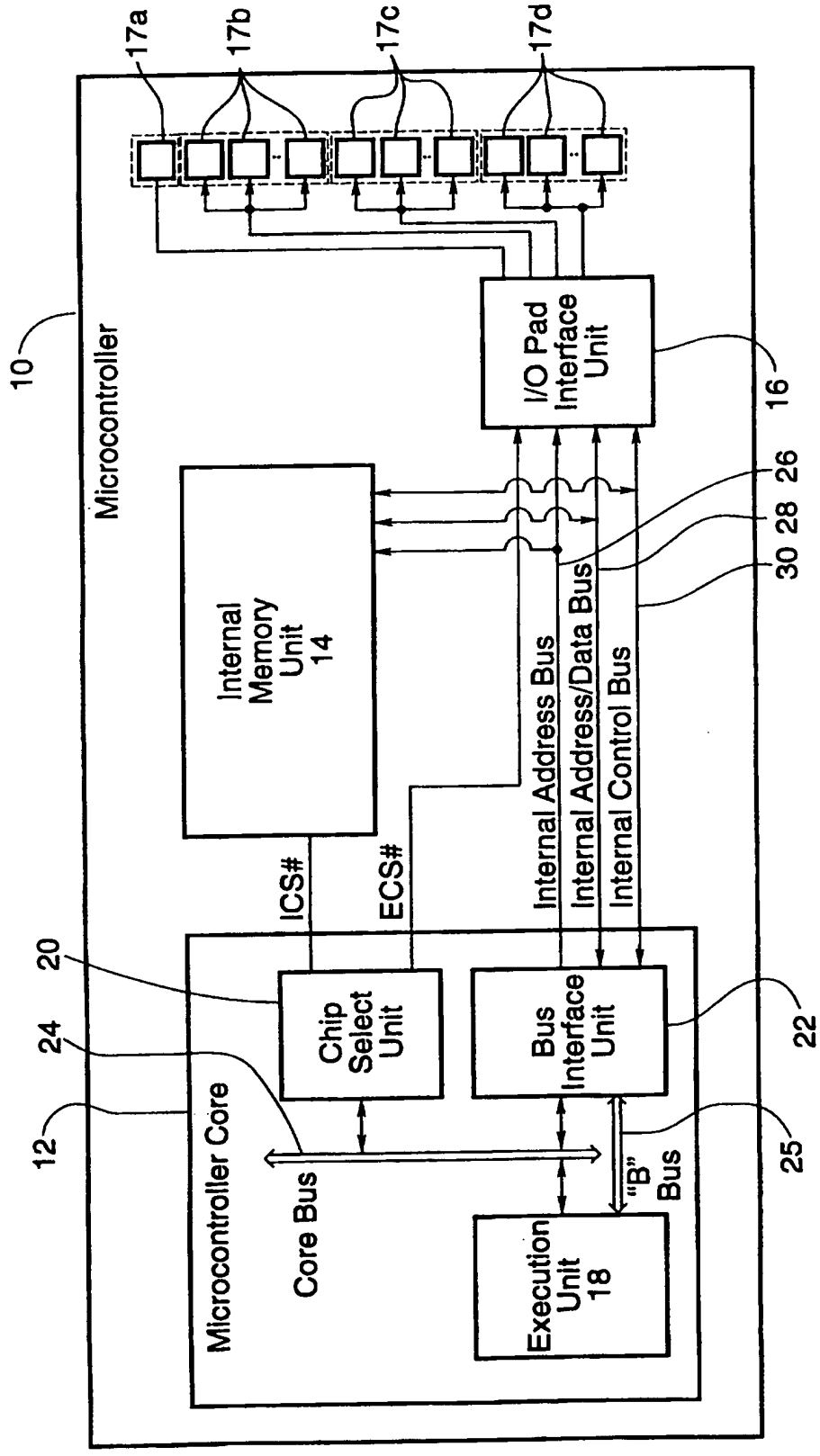

17a
17b
17c
17d
10
Microcontroller
I/O Pad Interface Unit
16
Internal Memory Unit 14
26
28
30
Internal Address Bus
Internal Address/Data Bus
Internal Control Bus
ICS#
ECS#
20
Chip Select Unit
Bus Interface Unit
22
24
12
Microcontroller Core
Core Bus
"B" Bus
25
Execution Unit 18

FIG. 1

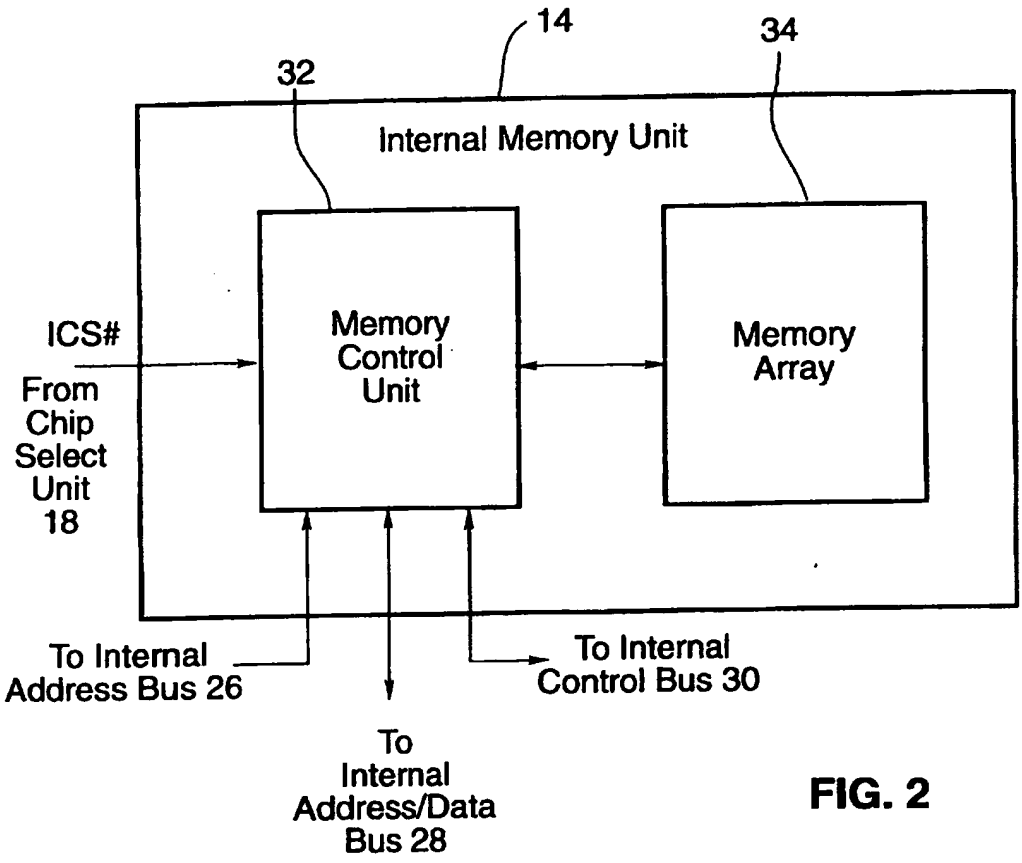

14
34
32
Internal Memory Unit
Memory Control Unit
Memory Array
ICS#
From Chip Select Unit 18
To Internal Address Bus 26
To Internal Control Bus 30
To Internal Address/Data Bus 28

FIG. 2

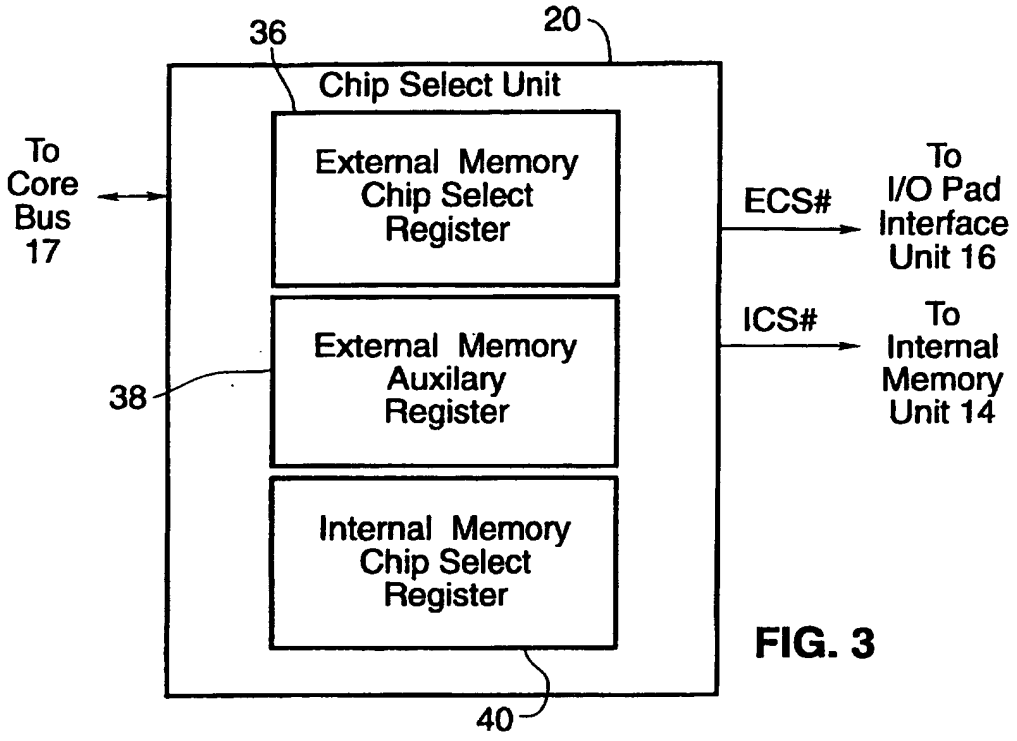
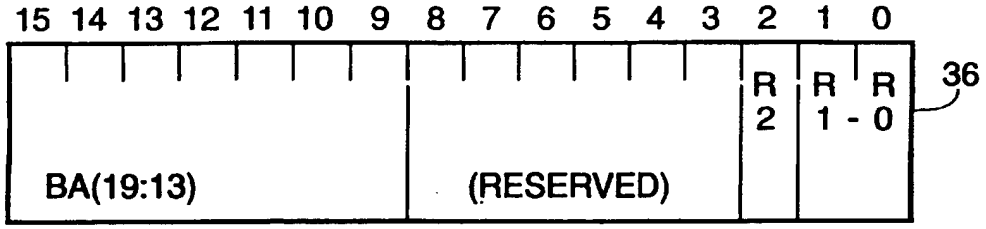


FIG. 3

FIG. 4



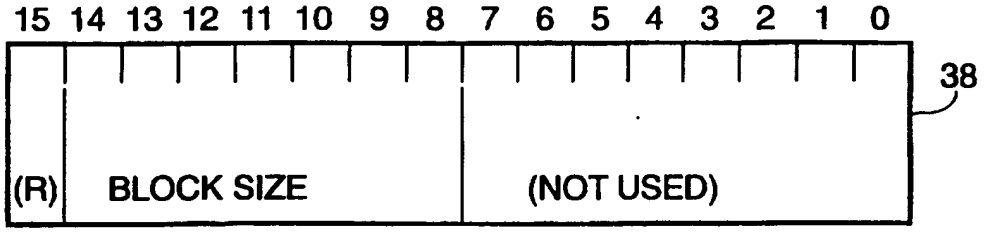


FIG. 5

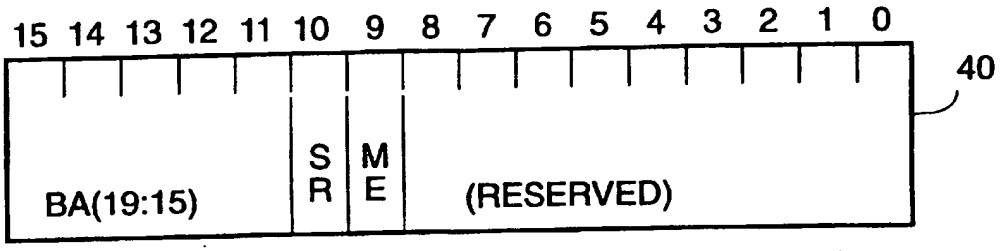

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
40
BA(19:15)
S R
M E
(RESERVED)

FIG. 6

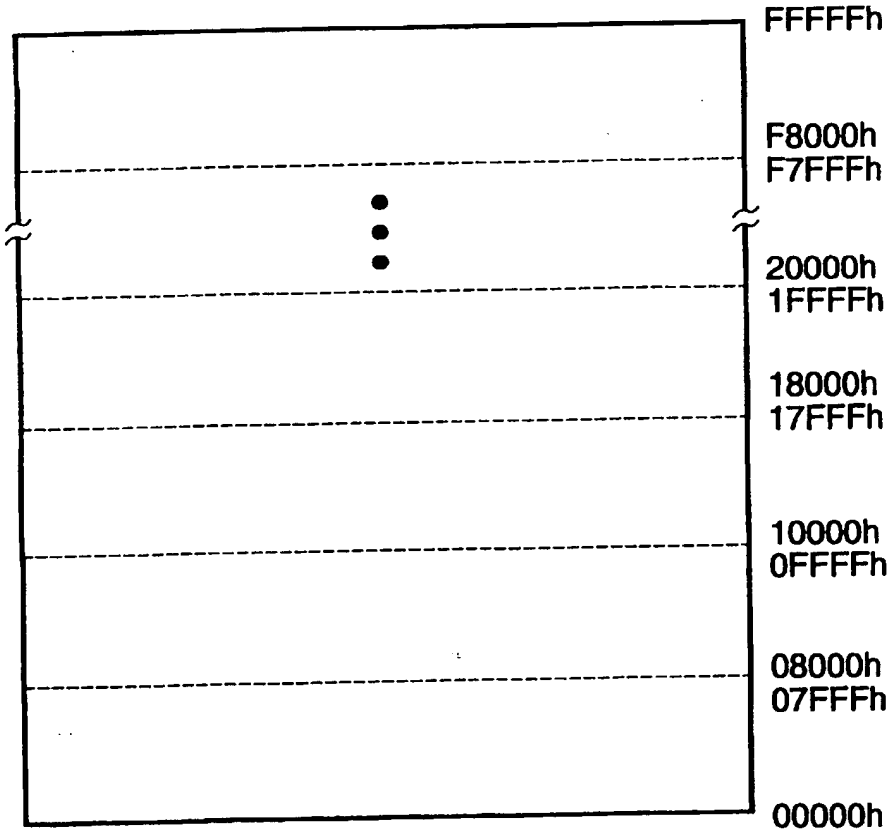

FFFFFh
F8000h
F7FFFh
20000h
1FFFFh
18000h
17FFFh
10000h
0FFFFh
08000h
07FFFh
00000h

FIG. 7

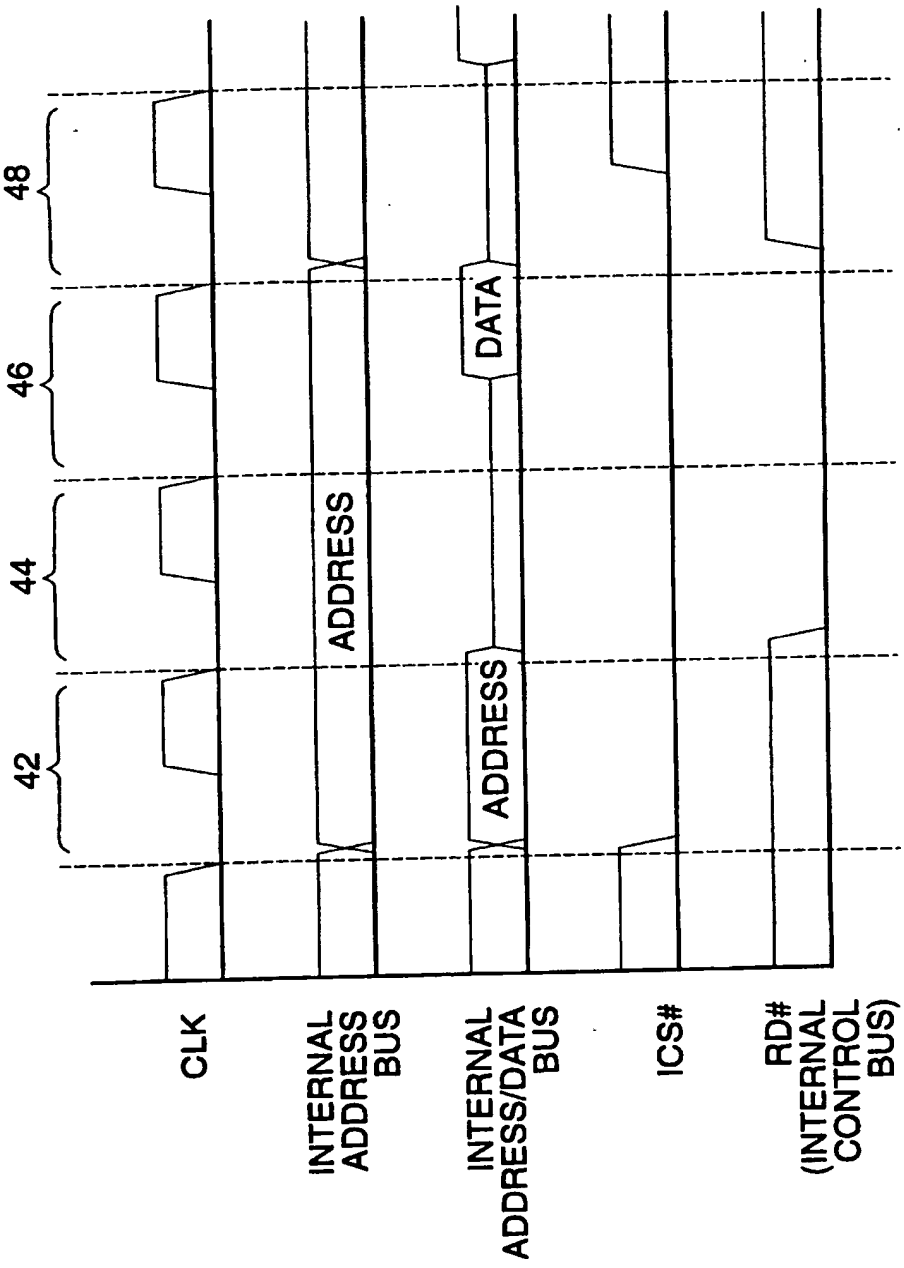

42
44
46
48
ADDRESS
ADDRESS
DATA
CLK
INTERNAL ADDRESS BUS
INTERNAL ADDRESS/DATA BUS
ICS#
RD# (INTERNAL CONTROL BUS)

FIG. 8

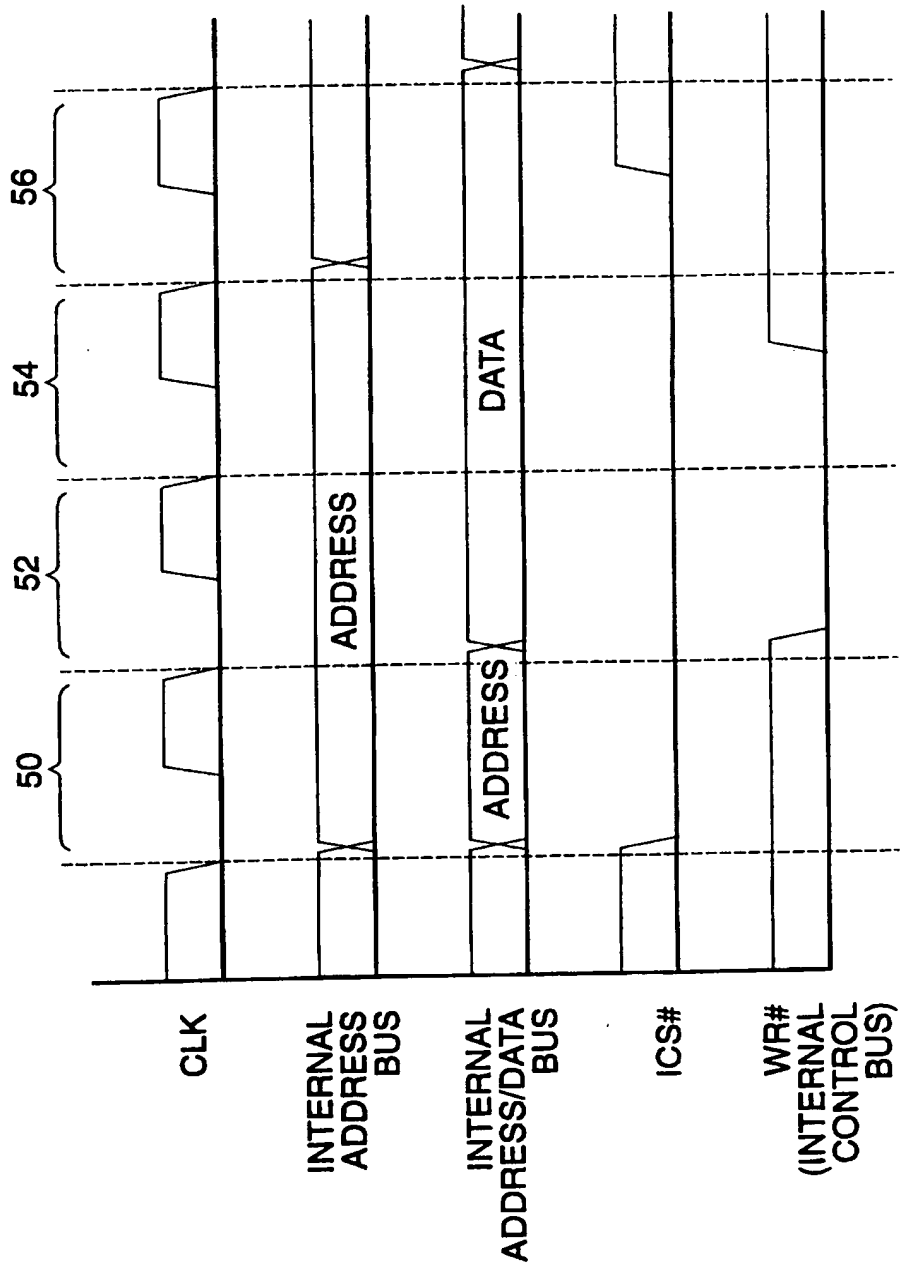

50
52
54
56
ADDRESS
DATA
ADDRESS
CLK
INTERNAL ADDRESS BUS
INTERNAL ADDRESS/DATA BUS
ICS#
WR# (INTERNAL CONTROL BUS)

FIG. 9

INTERNATIONAL SEARCH REPORT

Interr. ..al Application No
PCT/US 97/09545

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F15/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ANDREI R: "Free from the legacy of compatibility;microcontroller family with optimum price/performance ratio" ELEKTRONIK, 18 SEPT. 1987, WEST GERMANY, vol. 36, no. 19, ISSN 0013-5658, pages 99-100, 102, XP002041819 see the whole document ---	1,2,4, 17,19
A	US 5 438 681 A (MENSCH JR WILLIAM D) 1 August 1995 see column 5, line 16 - line 21 see column 5, line 65 - column 6, line 13 see column 11, line 35 - line 62 see column 12, line 3 - line 9; figure 3 --- -/--	1-26

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 September 1997	15. 10. 97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Michel, T

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INTERNATIONAL SEARCH REPORT

Interna al Application No
PCT/US 97/09545

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BURSKY D: "MICROCONTROLLER DESIGN EXPLOITS REUSABLE CORES WITH WORD WIDTHS OF 4 TO 32 BITS, CORE-BASED DESIGNS ENSURE OPTIMIZATION" ELECTRONIC DESIGN, vol. 42, no. 6, 21 March 1994, pages 53/54, 56, 58, 60-62, 66 - 68, XP000449354 see page 62, right-hand column, line 5 - page 66, left-hand column, line 3 ---	1,3,17, 18
A	EP 0 597 307 A (HITACHI LTD ;HITACHI MICROCOMPUTER SYST (JP); HITACHI VLSI ENG (JP) 18 May 1994 see the whole document ---	1,17
P,X	TYPALDOS M: "Using internal memory on the Am186ER microcontroller" EMBEDDED SYSTEM ENGINEERING, SEPT. 1996, ELECTRONIC DESIGN AUTOMATION, UK, vol. 4, no. 5, pages 50-52, XP002041820 see the whole document -----	1-26

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern. al Application No
PCT/US 97/09545

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5438681 A	01-08-95	NONE	
EP 0597307 A	18-05-94	JP 6150023 A	31-05-94
		US 5530965 A	25-06-96